What is claimed is:

1. A dual-port semiconductor memory device comprising:

a semiconductor substrate, which includes a memory cell having one N-well area where a p+-type active region is formed and one contiguous P-well area where an n+-type active region is formed;

a first word line;

a second word line (scan address line);

a first bit line;

a first complementary bit line;

a second bit line (scan data out line);

a first CMOS inverter, which includes a first NMOS transistor, a first PMOS transistor, an input terminal, and an output terminal;

a second CMOS inverter, which includes a second NMOS transistor, a second PMOS transistor, an input terminal, and an output terminal, wherein the input terminal of the second CMOS inverter is connected to the output terminal of the first CMOS inverter to form a first memory node and the output terminal of the second CMOS inverter is connected to the input terminal of the first CMOS inverter to form a second memory node;

a third NMOS transistor, which has a gate connected to the first word line, a drain connected to the first bit line, and a source connected to the first memory node;

a fourth NMOS transistor, which has a gate connected to the first word line, a drain connected to the first complementary bit line, and a source connected to the second memory node;

a fifth NMOS transistor, which has a gate connected to the first memory node and a source connected to a ground line; and

a sixth NMOS transistor, which has a gate connected to the second word line, a source connected to the drain of the fifth NMOS transistor, and a drain connected to the second bit line,

wherein the first PMOS transistor and the second PMOS transistor are disposed in the p+-type active region of the N-well area; and the first NMOS transistor, the second NMOS transistor, the third NMOS transistor, the fourth NMOS transistor, the fifth NMOS transistor, and the sixth NMOS transistor are formed in the

n+-type active region of the contiguous P-well area.

2. The dual-port semiconductor memory device of claim 1, wherein the N-well area is disposed at a corner of the memory cell, and the contiguous P-well area is disposed in a remaining portion of the memory cell.

3. The dual-port semiconductor memory device of claim 2, wherein a plurality of N-well areas constitute a common N-well area which is surrounded by the contiguous P-well area, and the dual-port semiconductor memory device further comprises a well contact used to connect the one common N-well area with a power source of the semiconductor memory device.

4. The dual-port semiconductor memory device of claim 3, wherein a second n+-type active region, which is connected to the well contact, is further formed in the p+-type active region of the common N-well area, and a silicide layer is formed in the second n+-type active region and the p+-type active region to connect the second n+-type active region and the p+-type active region to each other.

5. The dual-port semiconductor memory device of claim 3, wherein the common N-well area is shared by four memory cells.

6. The dual-port semiconductor memory device of claim 5, wherein the n+-type active region and the well contact in the p+-type active region are shared by two memory cells adjacent to each other.

7. The dual-port semiconductor memory device of claim 1, wherein an N-well bridge is further formed in the contiguous P-well area to connect N-well areas of memory cells that are adjacent to each other.

8. The dual-port semiconductor memory device of claim 7, wherein a width of the N-well bridge is 10% to 50% of a width of the N-well area.

9. The dual-port semiconductor memory device of claim 1, wherein the

second word line is parallel to the first word line.

10. The dual-port semiconductor memory device of claim 1, wherein the second bit line is parallel to the first bit line.

11. A dual-port semiconductor memory device comprising:

a semiconductor substrate, which includes a memory cell having one N-well area where a p+-type active region is formed and one contiguous P-well area where an n+-type active region is formed;

a first word line;

a second word line (scan address line);

a first bit line;

a first complementary bit line;

a second bit line (scan data out line);

a first CMOS inverter, which includes a first NMOS transistor, a first PMOS transistor, an input terminal, and an output terminal;

a second CMOS inverter, which includes a second NMOS transistor, a second PMOS transistor, an input terminal, and an output terminal, wherein the input terminal of the second CMOS inverter is connected to the output terminal of the first CMOS inverter to form a first memory node and the output terminal of the second CMOS inverter is connected to the input terminal of the first CMOS inverter to form a second memory node;

a third NMOS transistor, which has a gate connected to the first word line, a drain connected to the first bit line, and a source connected to the first memory node;

a fourth NMOS transistor, which has a gate connected to the first word line, a drain connected to the first complementary bit line, and a source connected to the second memory node; and

a fifth NMOS transistor, which has a gate connected to the second word line, a source connected to the first memory node, and a drain connected to the second bit line,

wherein the first PMOS transistor and the second PMOS transistor are disposed in the p+-type active region of the N-well area; and the first NMOS transistor, the second NMOS transistor, the third NMOS transistor, the fourth NMOS

transistor, and the fifth NMOS transistor are formed in the n+-type active region of the contiguous P-well area.

12. The dual-port semiconductor memory device of claim 11, wherein the N-well area is disposed at a corner of the memory cell, and the contiguous P-well area is disposed in a remaining portion of the memory cell.

13. The dual-port semiconductor memory device of claim 12, wherein a plurality of N-well areas constitute a common N-well area, which is surrounded by the contiguous P-well area, and the dual-port semiconductor memory device further comprises a well contact used to connect the one common N-well area with a power source of the semiconductor memory device.

14. The dual-port semiconductor memory device of claim 13, wherein a second n+-type active region, which is connected to the well contact, is further formed in the p+-type active region of the common N-well area, and a silicide layer is formed in the second n+-type active region and the p+-type active region to connect the second n+-type active region and the p+-type active region to each other.

15. The dual-port semiconductor memory device of claim 13, wherein the one common N-well area is shared by four memory cells.

16. The dual-port semiconductor memory device of claim 15, wherein the n+-type active region and the well contact in the p+-type active region are shared by two memory cells adjacent to each other.

17. The dual-port semiconductor memory device of claim 11, wherein an N-well bridge is further formed in the contiguous P-well area to connect the N-well areas of the memory cells adjacent to each other.

18. The dual-port semiconductor memory device of claim 17, wherein a width of the N-well bridge is 10% to 50% of a width of the N-well area.

19. The dual-port semiconductor memory device of claim 11, wherein the second word line is parallel to the first word line.

20. The dual-port semiconductor memory device of claim 11, wherein the second bit line is parallel to the first bit line.